Title: METHOD OF
MANUFACTURING
SEMICONDUCTOR DEVICES
Inventor(s): Sumio OGAWA et al.
Docket No.: 088941-0203

FIG. 1

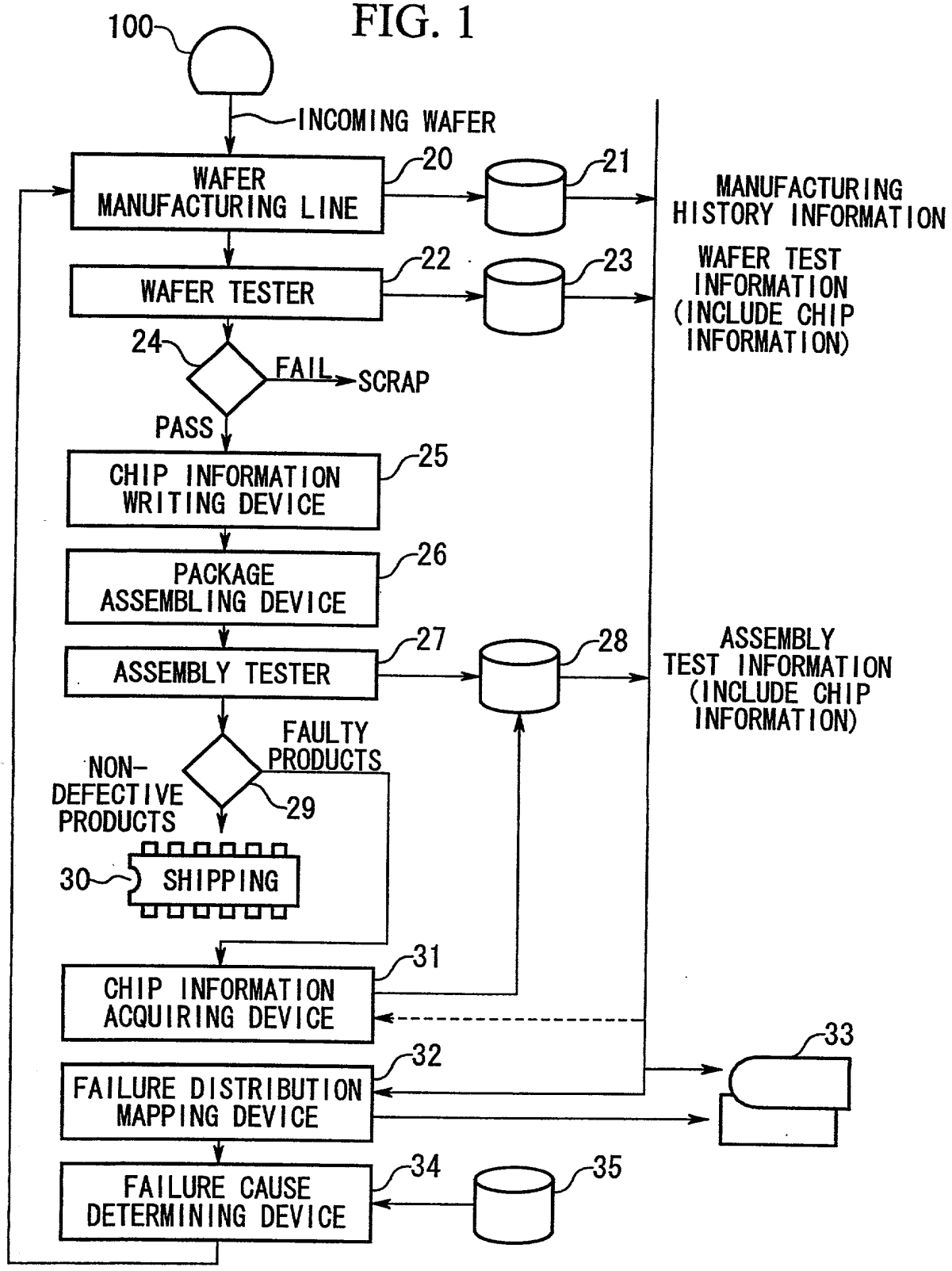


FIG. 2

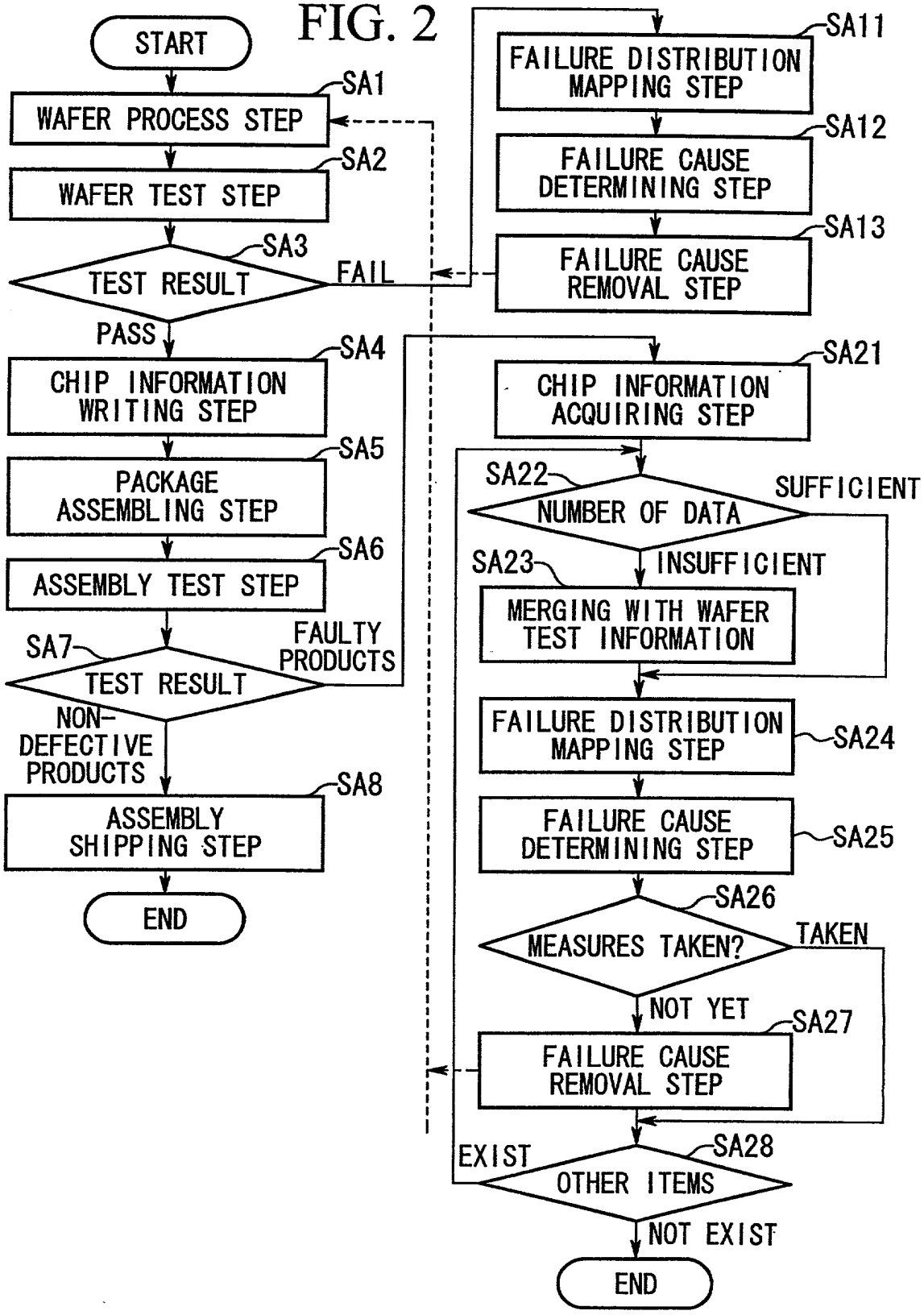

START
SA1
WAFER PROCESS STEP
SA2
WAFER TEST STEP
SA3
TEST RESULT
FAIL
PASS
SA4
CHIP INFORMATION WRITING STEP
SA5
PACKAGE ASSEMBLING STEP
SA6
ASSEMBLY TEST STEP
SA7
TEST RESULT
FAULTY PRODUCTS
NON-DEFECTIVE PRODUCTS
SA8
ASSEMBLY SHIPPING STEP
END
SA11
FAILURE DISTRIBUTION MAPPING STEP
SA12
FAILURE CAUSE DETERMINING STEP
SA13
FAILURE CAUSE REMOVAL STEP
SA21
CHIP INFORMATION ACQUIRING STEP
SA22
NUMBER OF DATA
SUFFICIENT
INSUFFICIENT
SA23
MERGING WITH WAFER TEST INFORMATION
FAILURE DISTRIBUTION MAPPING STEP
SA24
FAILURE CAUSE DETERMINING STEP
SA25
SA26
MEASURES TAKEN?
TAKEN
NOT YET
SA27
FAILURE CAUSE REMOVAL STEP
EXIST
SA28
OTHER ITEMS
NOT EXIST
END

FIG. 3

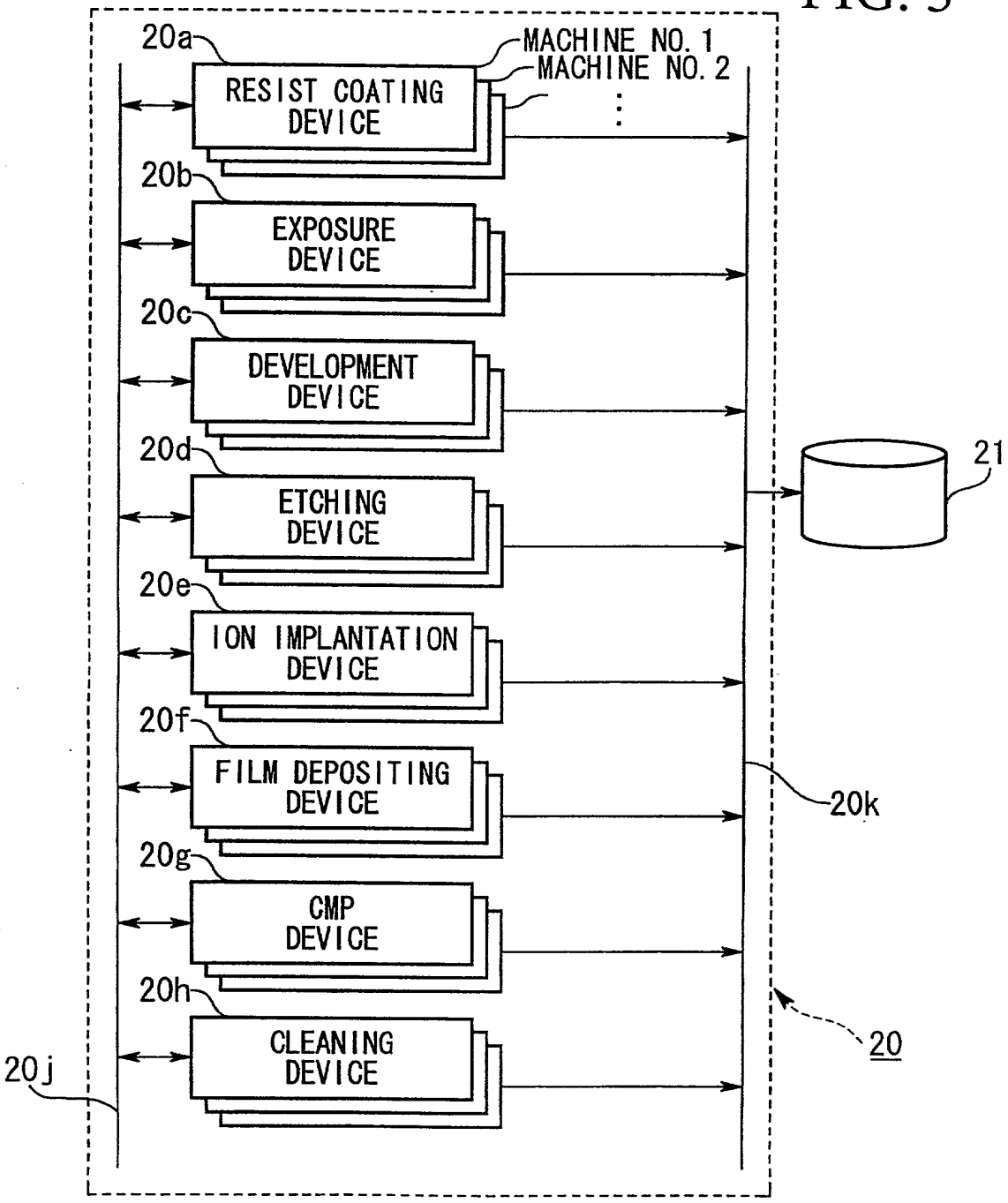

20a
MACHINE NO. 1
MACHINE NO. 2
RESIST COATING DEVICE
20b
EXPOSURE DEVICE
20c
DEVELOPMENT DEVICE
20d
ETCHING DEVICE
20e
ION IMPLANTATION DEVICE
20f
FILM DEPOSITING DEVICE
20g
CMP DEVICE
20h
CLEANING DEVICE
20j
21
20k
20

FIG. 4

PRODUCT NAME	LOT NUMBER	WAFER NUMBER	STEP NAME	MANUFACTURING TIME AND DATE	MANUFACTURING MACHINE NO.	MANUFACTURING CONDITION
UPD123	CB95-3030	W01	STEP A	20000101	MACHINE NO. H5	5021
			STEP B	20000102	MACHINE NO. L3	4791
			...	...	...	...
		W02	STEP A	20000101	MACHINE NO. H6	5021
			STEP B	20000102	MACHINE NO. L7	4791
			...	...	...	...
		...	...	...	...	...
	...	...	...	...	...	...
...						

FIG. 5

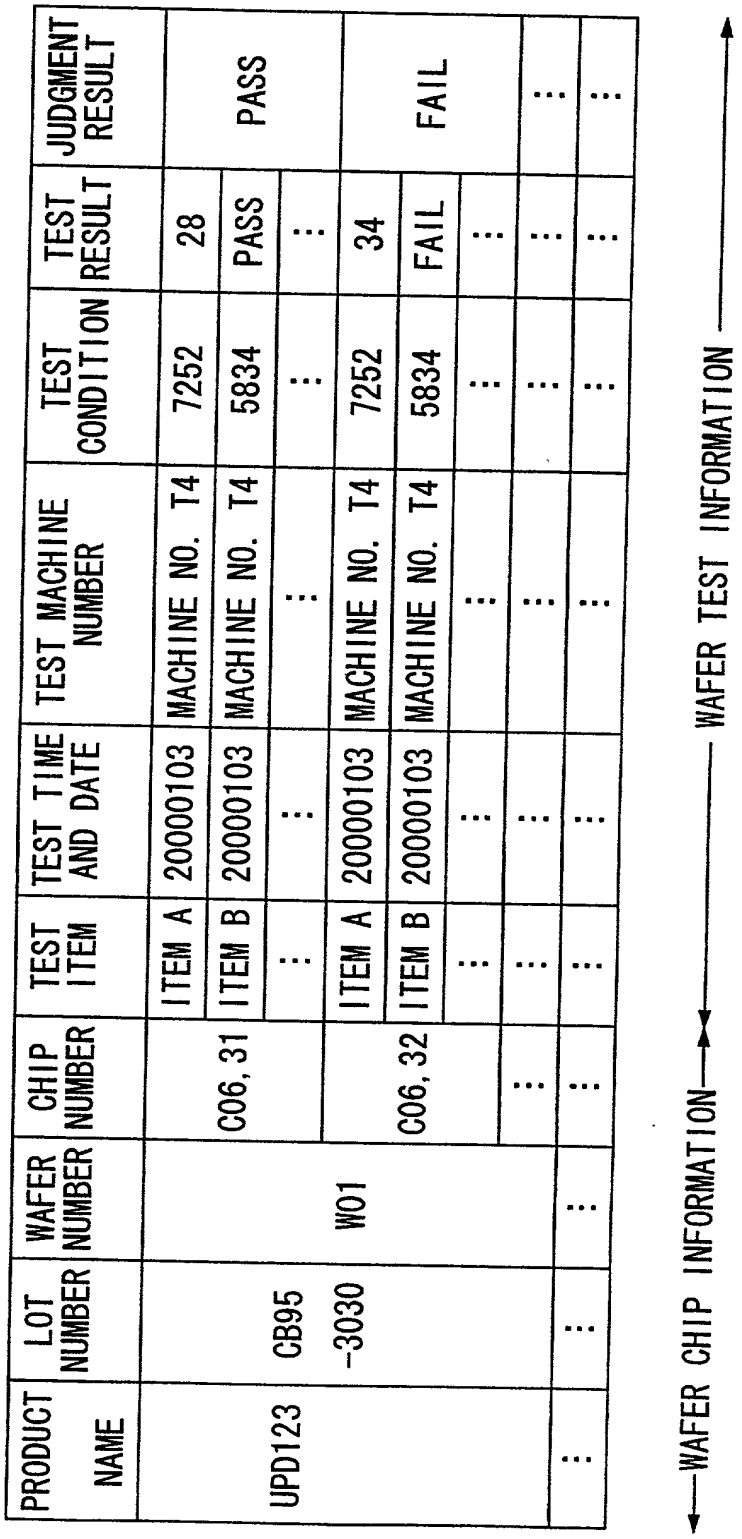

PRODUCT NAME
LOT NUMBER
WAFER NUMBER
CHIP NUMBER
TEST ITEM
TEST TIME AND DATE
TEST MACHINE NUMBER
TEST CONDITION
TEST RESULT
JUDGMENT RESULT
UPD123
CB95 -3030
W01
C06, 31
C06, 32
ITEM A
ITEM B
20000103
MACHINE NO. T4
7252
5834
28
34
PASS
FAIL
WAFER CHIP INFORMATION
WAFER TEST INFORMATION

FIG. 6A

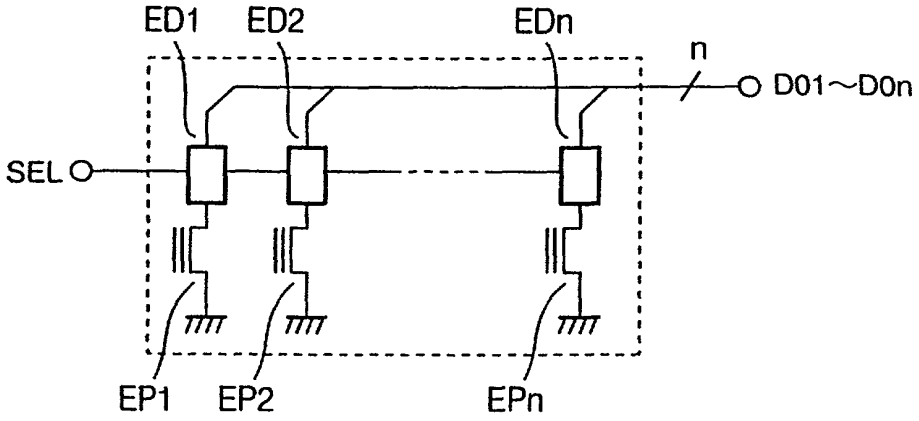

ED1
ED2
EDn
n
D01~D0n
SEL
EP1
EP2
EPn

FIG. 6B

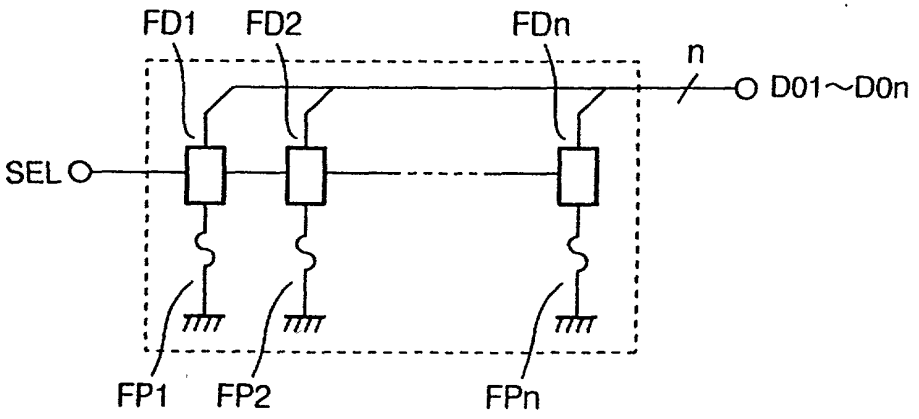

FD1
FD2
FDn
n
D01~D0n
SEL
FP1
FP2
FPn

FIG. 7

PRODUCT NAME	LOT NUMBER	ASSEMBLY LOT NUMBER	WAFER NUMBER	CHIP NUMBER	SAMPLE NUMBER	TEST ITEM	TEST TIME AND DATE	TEST MACHINE NUMBER	TEST CONDITION	TEST RESULT	JUDGMENT RESULT
UPD123	CB95 -3030	35ER-008	W01	C06, 31	007	ITEM K	20000107	MACHINE NO. H2	7251	27	FAIL
						ITEM L	20000107	MACHINE NO. H2	5832	FAIL	
						⋮	⋮	⋮	⋮	⋮	
				—	—	ITEM K	20000107	MACHINE NO. H2	7251	26	PASS
						ITEM L	20000107	MACHINE NO. H2	5832	PASS	
						⋮	⋮	⋮	⋮	⋮	
				⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮

← ASSEMBLY CHIP INFORMATION → ← ASSEMBLY TEST INFORMATION →

FIG. 8

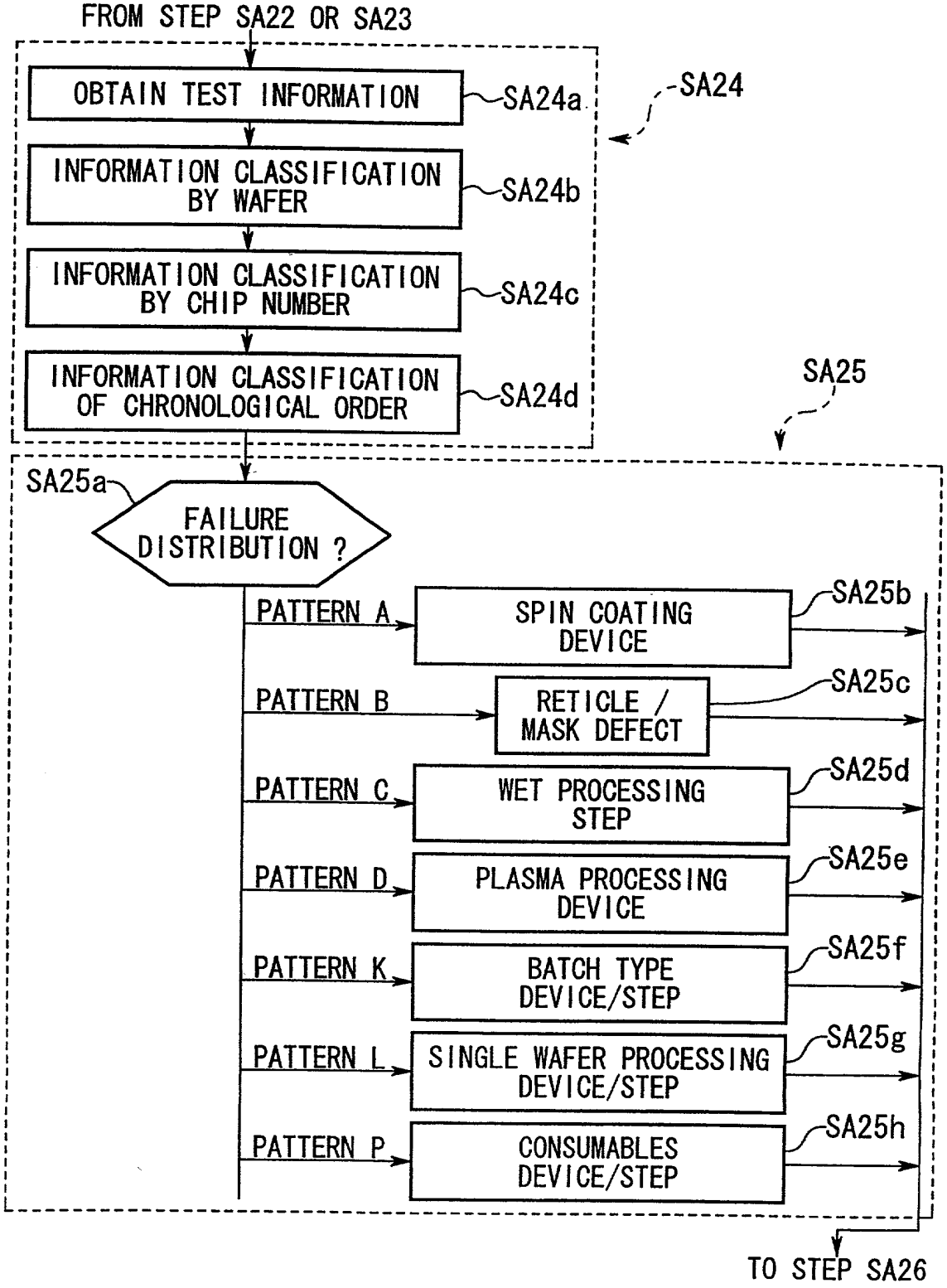

FROM STEP SA22 OR SA23
OBTAIN TEST INFORMATION
SA24a
SA24
INFORMATION CLASSIFICATION BY WAFER
SA24b
INFORMATION CLASSIFICATION BY CHIP NUMBER
SA24c
INFORMATION CLASSIFICATION OF CHRONOLOGICAL ORDER
SA24d
SA25
SA25a
FAILURE DISTRIBUTION ?
PATTERN A
SPIN COATING DEVICE
SA25b
PATTERN B
RETICLE / MASK DEFECT
SA25c
PATTERN C
WET PROCESSING STEP
SA25d
PATTERN D
PLASMA PROCESSING DEVICE
SA25e
PATTERN K
BATCH TYPE DEVICE/STEP
SA25f
PATTERN L
SINGLE WAFER PROCESSING DEVICE/STEP
SA25g
PATTERN P
CONSUMABLES DEVICE/STEP
SA25h
TO STEP SA26

FIG. 9

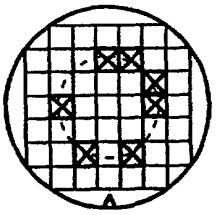
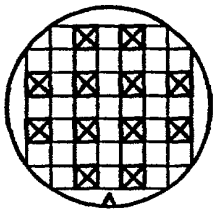
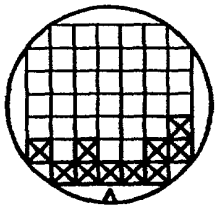
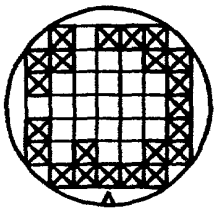
	FAILURE DISTRIBUTION PATTERN	FAILURE CAUSE	IMPROVEMENT AREA
A		WHEN PROCESSING SOLVENT IS COATED ON ROTATING WAFER, LIQUID LEFT IN NOZZLE DRIPS AND MAKES FILM THICKNESS INCONSISTENT, AND HENCE CONTACT FAILURE OCCURS.	·RESIST COATING DEVICE ·SOG FILM DEPOSITING DEVICE
B		WHEN A PLURALITY OF CHIPS IS EXPOSED AT THE SAME TIME IN RETICLE, IF A PART OF RETICLE IS DEFECTIVE, FAILURES OCCUR AT A SPECIFIC LOCATION IN EACH EXPOSURE.	·RETICLE
C		WHEN VERTICALLY MOUNTED WAFER IS IMMERSED IN PROCESSING LIQUID, DIFFERENCE IN PROCESSING TIME OCCURS BETWEEN UPPER AND LOWER PART OF THE WAFER, AND HENCE FAILURES OCCUR CONCENTRATED IN THE UPPER PART OR LOWER PART.	·WET ETCHING DEVICE /STEP ·BATCH TYPE CLEANING DEVICE /STEP
D		IN THE PLASMA ETCHING DEVICE, ELECTRIC FIELD BECOMES INCONSISTENT IN THE PERIPHERY OF THE WAFER, AND HENCE FAILURES OCCUR IN THE PERIPHERY OF THE WAFER.	·PLASMA PROCESSING DEVICE
⋮	⋮	⋮	⋮

FIG.10

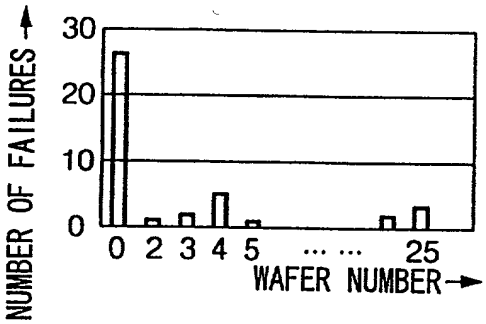
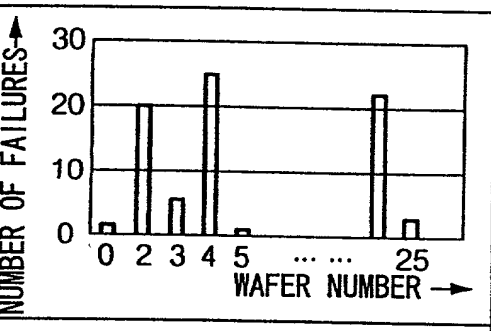
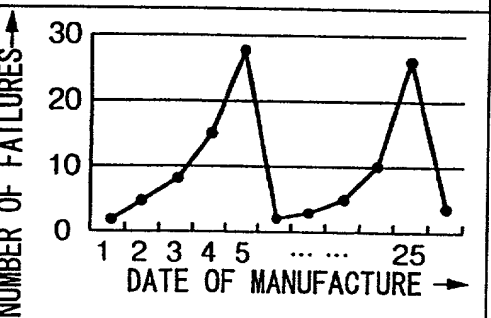
	FAILURE DISTRIBUTION PATTERN	FAILURE CAUSE	IMPROVEMENT AREA
K		IN BATCH TYPE PROCESS STEP, PROCESSING LIQUID /GAS BECOMES INCONSISTENT BETWEEN THE FIRST WAFER AND THE SECOND AND LATER WAFERS SO THAT FAILURES OCCUR FREQUENTLY ONLY ON THE FIRST WAFER.	·BATCH TYPE WET ETCHING DEVICE/STEP ·BATCH TYPE THERMAL DIFFUSION DEVICE/STEP ·BATCH TYPE THERMAL OXIDATION DEVICE/STEP ·FURNACE TUBE
L		IN SINGLE WAFER TYPE PROCESSING DEVICE, IF A SPECIFIC MACHINE IS FAULTY, FAILURES OCCUR FREQUENTLY FOR THE MACHINE NUMBER.	·SINGLE WAFER TYPE CVD DEVICE/STEP ·SINGLE WAFER TYPE EXPOSURE DEVICE/STEP ·SINGLE WAFER TYPE ETCHING DEVICE/STEP
⋮	⋮	⋮	⋮
P		IN A SPECIFIC TEST ITEM AND MANUFACTURING DEVICE, IF THERE IS ABRASION AND THE LIKE IN THE EQUIPMENT, FAILURE RATE INCREASES OVER TIME.	·VACUUM PACKING EQUIPMENT ·OBSOLESCENCE OF LIQUID IN PROCESS WITH RECIRCULATING ETCHING LIQUID ·SENSITIVITY OF SENSOR DROP
⋮	⋮	⋮	⋮

FIG. 11

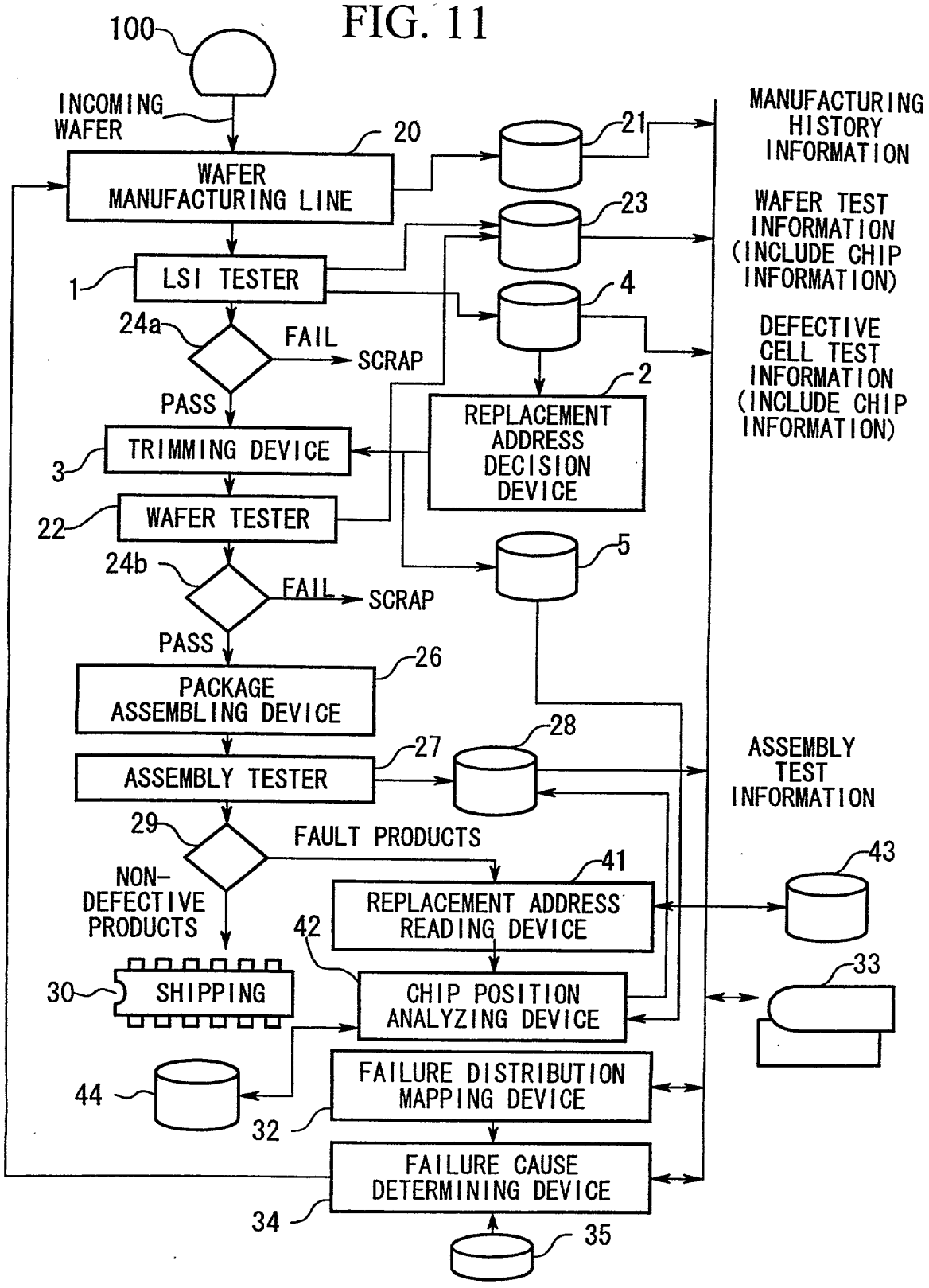

100
INCOMING WAFER
WAFER MANUFACTURING LINE
20
21
MANUFACTURING HISTORY INFORMATION
23
WAFER TEST INFORMATION (INCLUDE CHIP INFORMATION)
1
LSI TESTER
4
DEFECTIVE CELL TEST INFORMATION (INCLUDE CHIP INFORMATION)
24a
FAIL
SCRAP
PASS
2
REPLACEMENT ADDRESS DECISION DEVICE
3
TRIMMING DEVICE
22
WAFER TESTER
5
24b
FAIL
SCRAP
PASS
26
PACKAGE ASSEMBLING DEVICE
28
27
ASSEMBLY TESTER
ASSEMBLY TEST INFORMATION
29
FAULT PRODUCTS
NON-DEFECTIVE PRODUCTS
41
43
REPLACEMENT ADDRESS READING DEVICE
42
30
SHIPPING
CHIP POSITION ANALYZING DEVICE
33
44
FAILURE DISTRIBUTION MAPPING DEVICE
32
FAILURE CAUSE DETERMINING DEVICE
34
35

FIG. 12

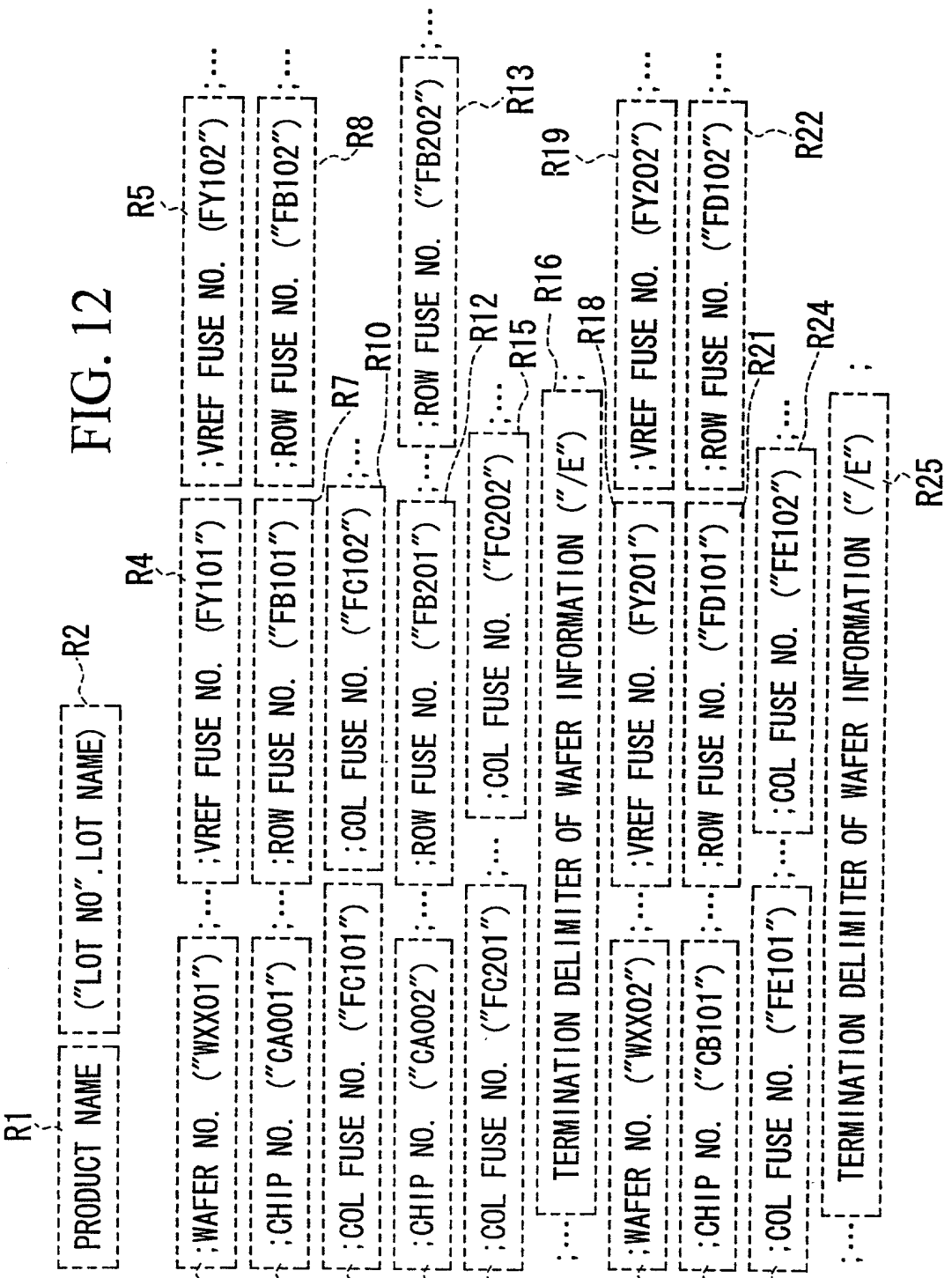

R1
PRODUCT NAME ("LOT NO".LOT NAME)
R2
R3
;WAFER NO. ("WXX01") ;... ;VREF FUSE NO. (FY101") ;... ;VREF FUSE NO. (FY102") ;...
R4
R5
R6
;CHIP NO. ("CA001") ;... ;ROW FUSE NO. ("FB101") ;... ;ROW FUSE NO. ("FB102") ;...
R7
R8
R9
;COL FUSE NO. ("FC101") ;... ;COL FUSE NO. ("FC102") ;...
R10
R11
;CHIP NO. ("CA002") ;... ;ROW FUSE NO. ("FB201") ;... ;ROW FUSE NO. ("FB202") ;...
R12
R13
R14
;COL FUSE NO. ("FC201") ;... ;COL FUSE NO. ("FC202") ;...
R15
R16
R17
;... TERMINATION DELIMITER OF WAFER INFORMATION ("/E") ;...
R18
R19
;WAFER NO. ("WXX02") ;... ;VREF FUSE NO. (FY201") ;... ;VREF FUSE NO. (FY202") ;...
R20
;CHIP NO. ("CB101") ;... ;ROW FUSE NO. ("FD101") ;... ;ROW FUSE NO. ("FD102") ;...
R21
R22
R23
;COL FUSE NO. ("FE101") ;... ;COL FUSE NO. ("FE102") ;...
R24
;... TERMINATION DELIMITER OF WAFER INFORMATION ("/E") ;...
R25

FIG. 13

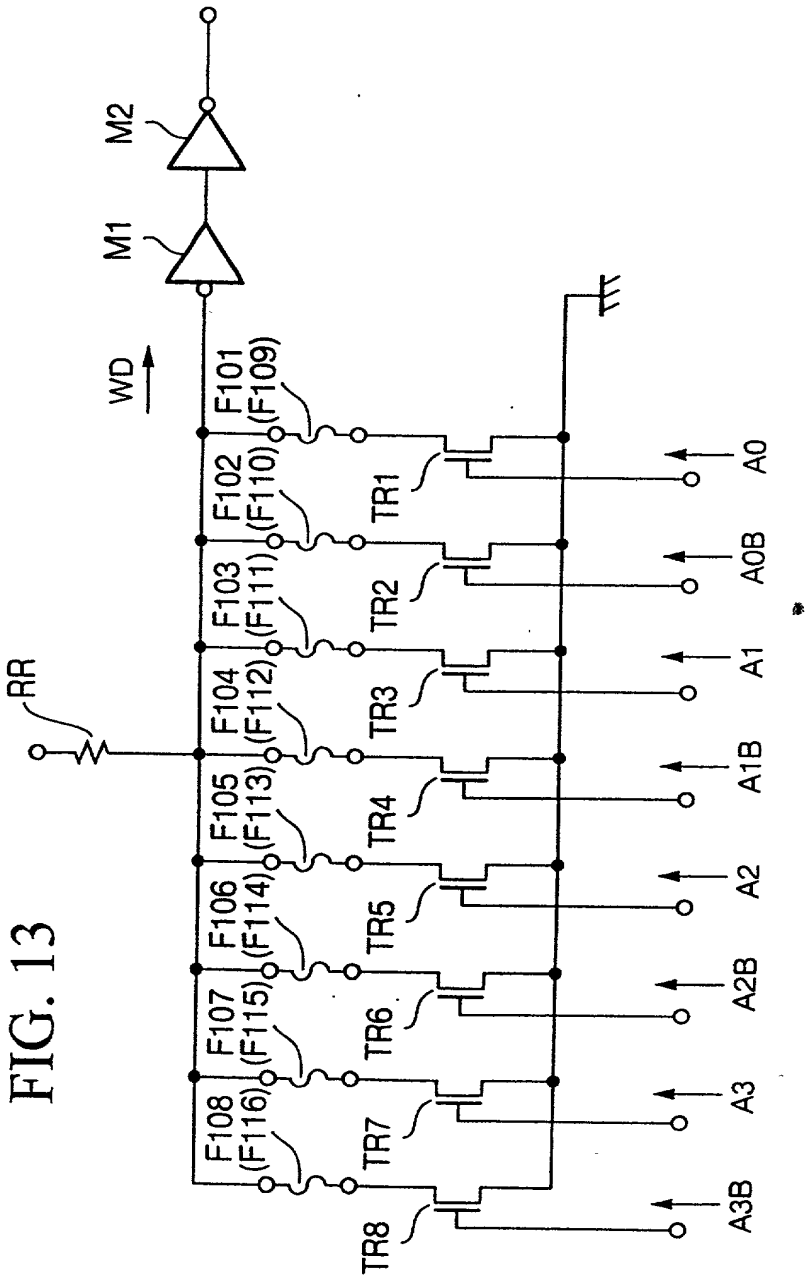

M2
M1
WD
RR
F101 (F109)
F102 (F110)
F103 (F111)
F104 (F112)
F105 (F113)
F106 (F114)
F107 (F115)
F108 (F116)
TR1
TR2
TR3
TR4
TR5
TR6
TR7
TR8
A0
A0B
A1
A1B
A2
A2B
A3
A3B

FIG. 14

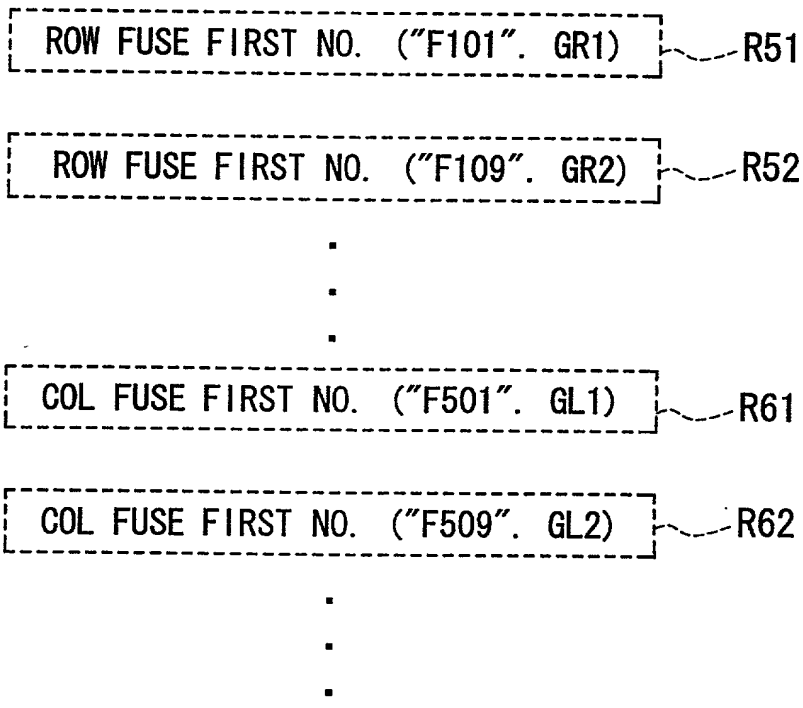
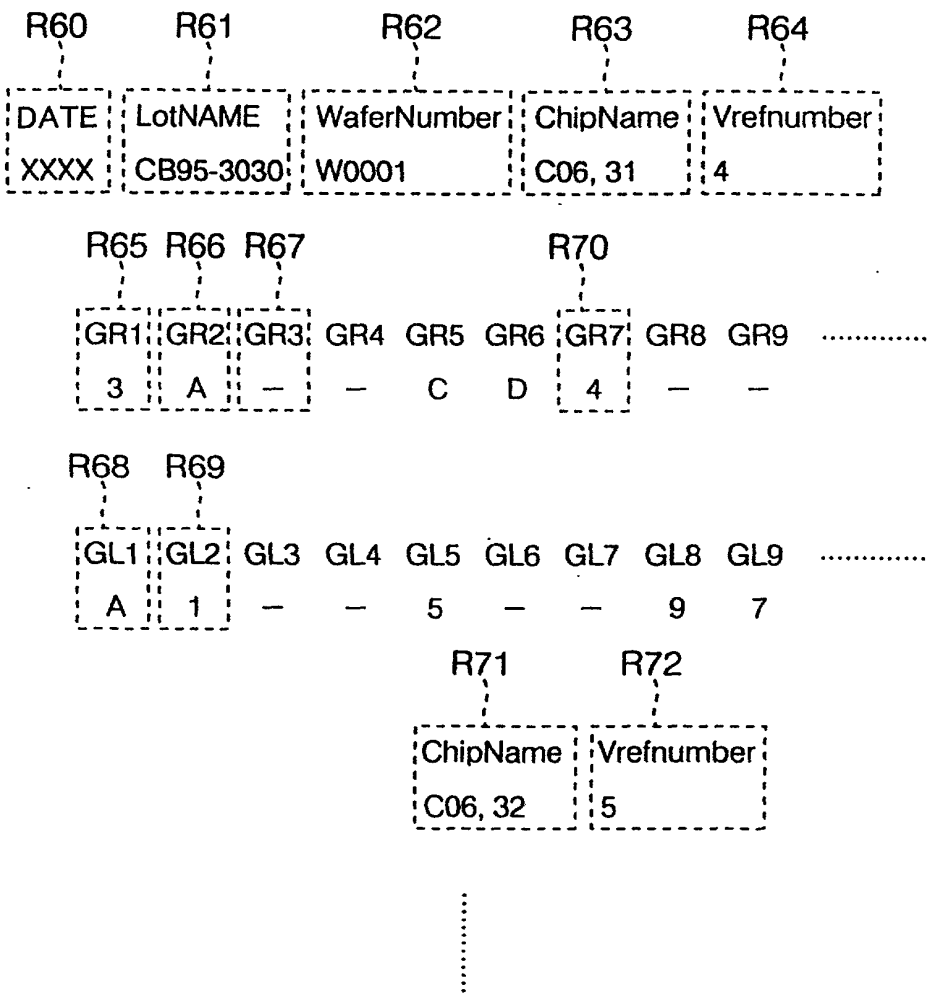

ROW FUSE FIRST NO. ("F101". GR1)
R51
ROW FUSE FIRST NO. ("F109". GR2)
R52
COL FUSE FIRST NO. ("F501". GL1)
R61
COL FUSE FIRST NO. ("F509". GL2)
R62

FIG. 15

PRODUCT NAME
LOT NAME ("LOT NO", CB95-3030)
WAFER NO. ("W0001")
VREF FUSE NO. ("FY101")
VREF FUSE NO. ("FY102")
⋮
CHIP NO. ("CA001")
ROW FUSE NO. ("F101")
ROW FUSE NO. ("F103")
ROW FUSE NO. ("F106")
ROW FUSE NO. ("F108")
ROW FUSE NO. ("F110")
ROW FUSE NO. ("F113")
ROW FUSE NO. ("F114")
ROW FUSE NO. ("F115")
⋮
COL FUSE NO. ("F501")
COL FUSE NO. ("F503")
COL FUSE NO. ("F506")
COL FUSE NO. ("F507")
COL FUSE NO. ("F509")
COL FUSE NO. ("F512")
COL FUSE NO. ("F514")
COL FUSE NO. ("F516")
⋮
TERMINATION DELIMITER OF WAFER INFORMATION ("/E")
⋮

FIG. 16


R60
R61
R62
R63
R64
DATE
XXXX
LotNAME
CB95-3030
WaferNumber
W0001
ChipName
C06, 31
Vrefnumber
4
R65
R66
R67
R70
GR1
3
GR2
A
GR3
–
GR4
–
GR5
C
GR6
D
GR7
4
GR8
–
GR9
–
R68
R69
GL1
A
GL2
1
GL3
–
GL4
–
GL5
5
GL6
–
GL7
–
GL8
9
GL9
7
R71
R72
ChipName
C06, 32
Vrefnumber
5

Title: METHOD OF
MANUFACTURING
SEMICONDUCTOR DEVICES
Inventor(s): Sumio OGAWA et al.
Docket No.: 088941-0203

FIG. 17

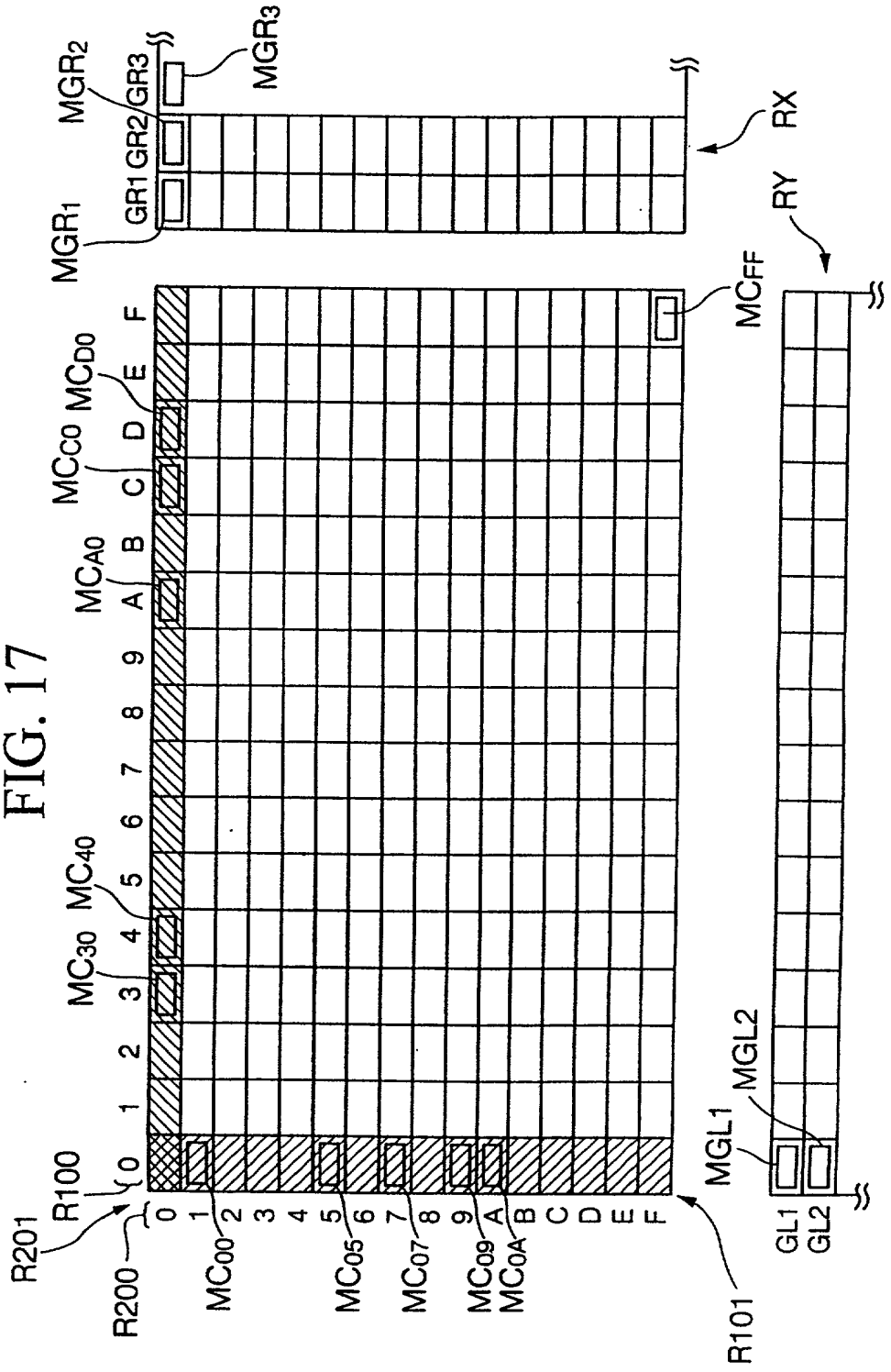


FIG. 18

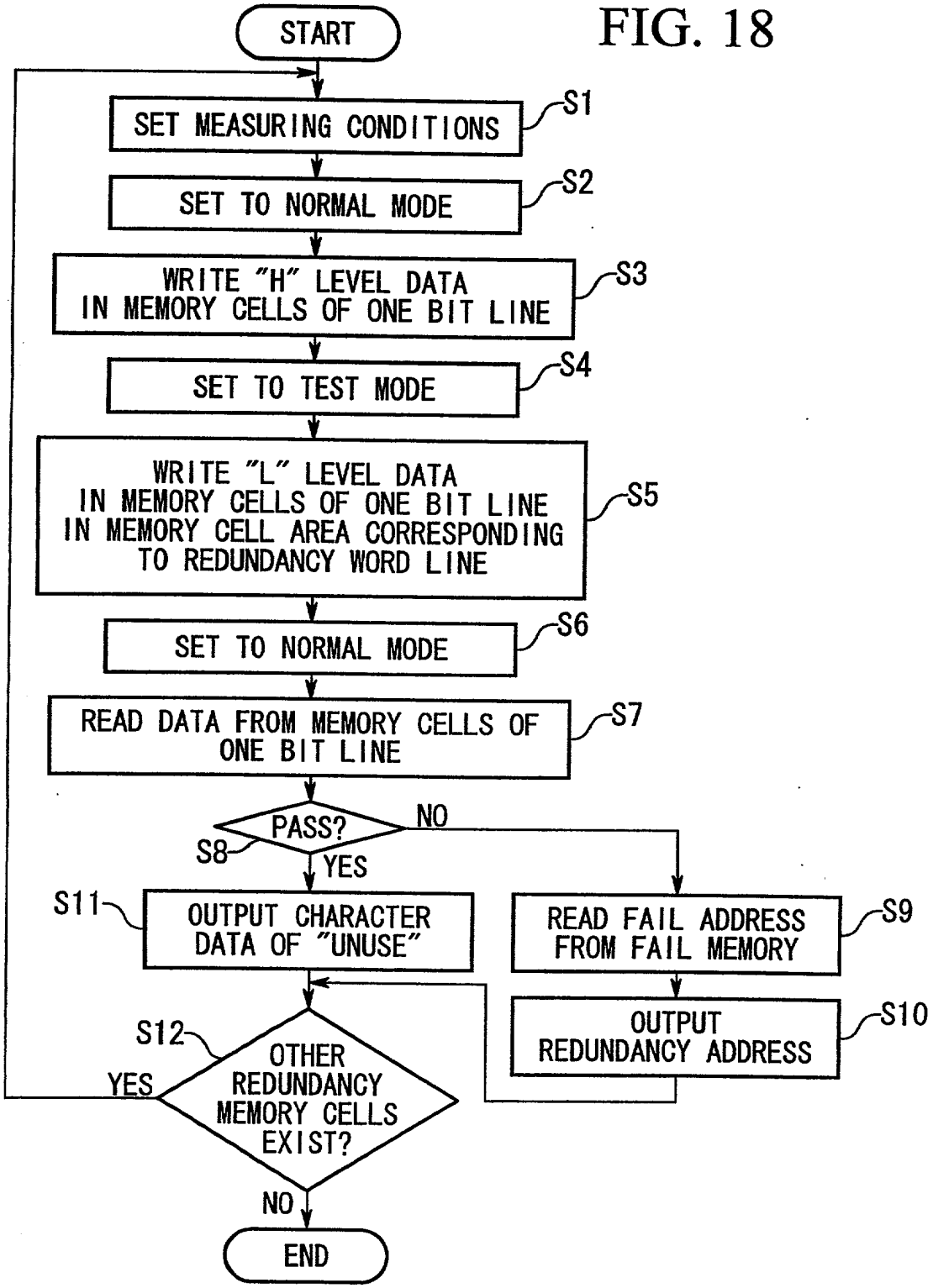

START
SET MEASURING CONDITIONS
S1
SET TO NORMAL MODE
S2
WRITE "H" LEVEL DATA IN MEMORY CELLS OF ONE BIT LINE
S3
SET TO TEST MODE
S4
WRITE "L" LEVEL DATA IN MEMORY CELLS OF ONE BIT LINE IN MEMORY CELL AREA CORRESPONDING TO REDUNDANCY WORD LINE
S5
SET TO NORMAL MODE
S6
READ DATA FROM MEMORY CELLS OF ONE BIT LINE
S7
PASS?
S8
NO
YES
S11
OUTPUT CHARACTER DATA OF "UNUSE"
READ FAIL ADDRESS FROM FAIL MEMORY
S9
OUTPUT REDUNDANCY ADDRESS
S10
S12
OTHER REDUNDANCY MEMORY CELLS EXIST?
YES
NO
END

FIG. 19

X-Redundancy RoLL C

FUSE	REDUNDANCY ADDRESS	
F101 ~F108	3	R301
F109 ~F116	A	R302
F117~F124	UNUSE	R303

Y-Redundancy RoLL C

FUSE	REDUNDANCY ADDRESS	
F501 ~F508	A	R351
F509 ~F516	1	
F517 ~F524	UNUSE	

FIG. 20

R401	R402	R403	R404	R505
WAFER STEP LOT NO	ASSEMBLY LOT NO	WAFER NO	CHIP NO	SAMPLE NO
CB95-3030	35er008	W01	C06, 31	1
CB95-3030	35er008	W01	C06, 32	2

FIG. 21

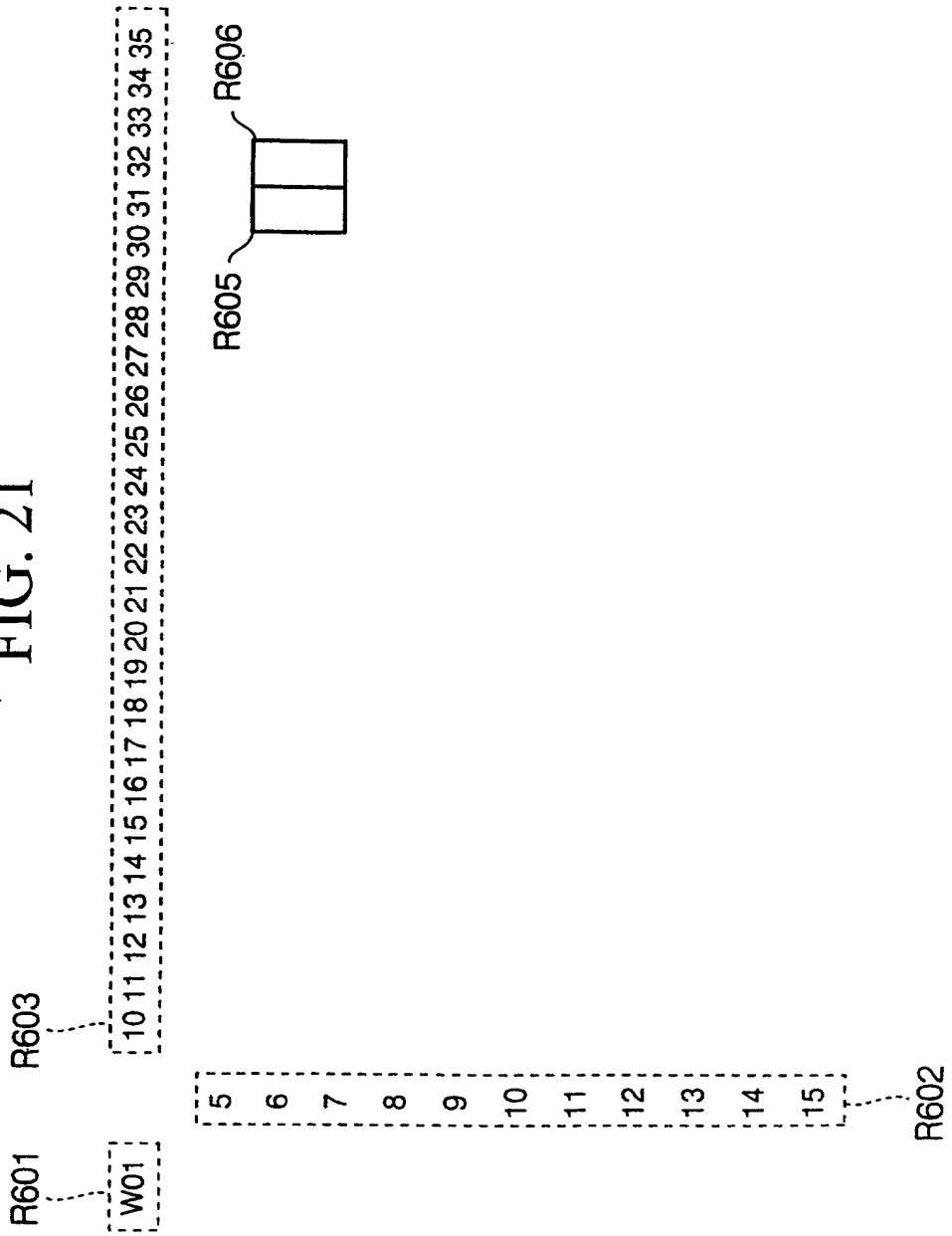

R601
W01
R603
10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35
R605
R606
5 6 7 8 9 10 11 12 13 14 15
R602

FIG. 22

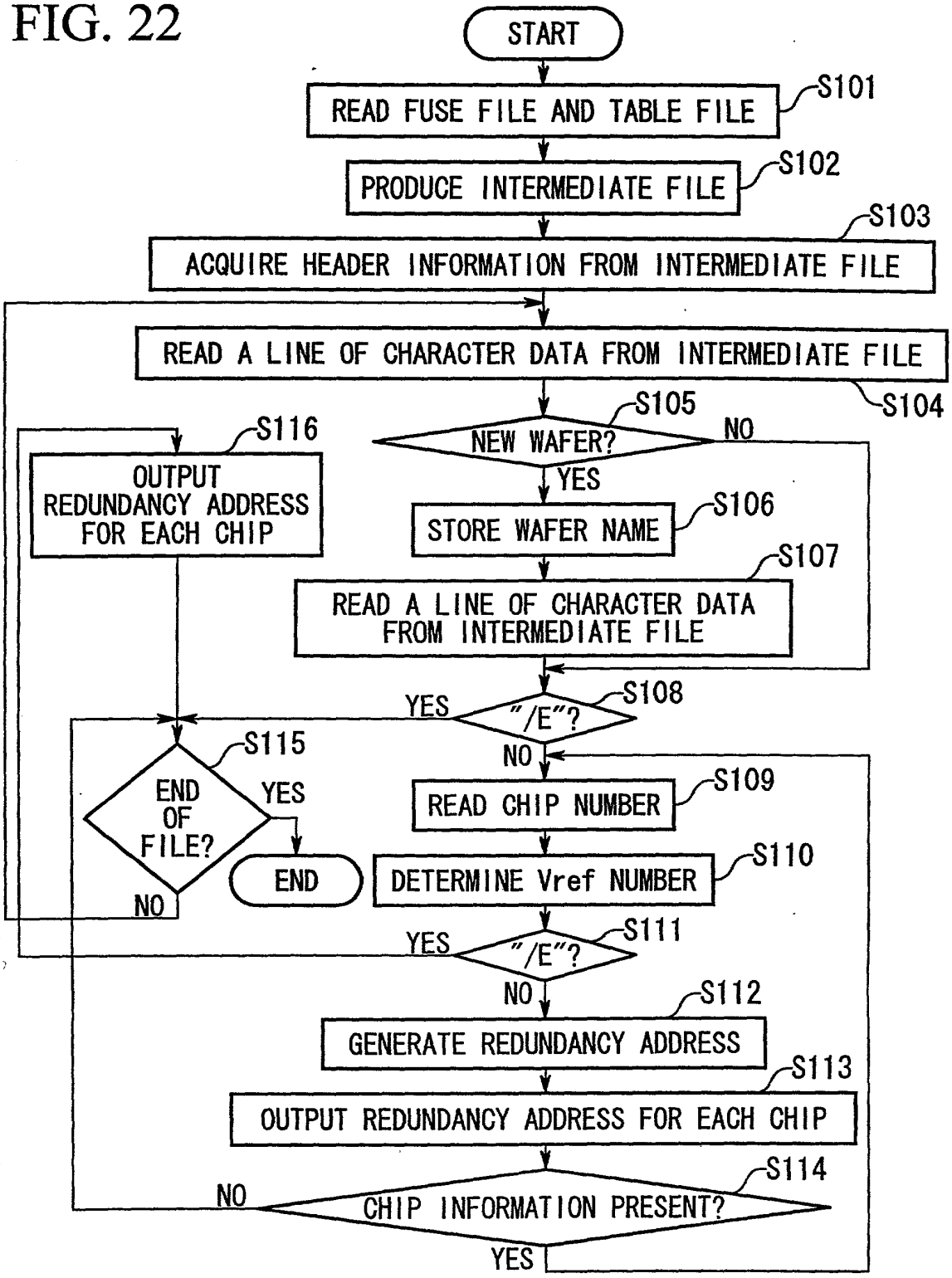

START
READ FUSE FILE AND TABLE FILE
S101
PRODUCE INTERMEDIATE FILE
S102
ACQUIRE HEADER INFORMATION FROM INTERMEDIATE FILE
S103
READ A LINE OF CHARACTER DATA FROM INTERMEDIATE FILE
S104
NEW WAFER?
S105
NO
YES
STORE WAFER NAME
S106
READ A LINE OF CHARACTER DATA FROM INTERMEDIATE FILE
S107
"/E"?
S108
YES
NO
READ CHIP NUMBER
S109
DETERMINE Vref NUMBER
S110
"/E"?
S111
YES
NO
GENERATE REDUNDANCY ADDRESS
S112
OUTPUT REDUNDANCY ADDRESS FOR EACH CHIP
S113
CHIP INFORMATION PRESENT?
S114
NO
YES
END OF FILE?
S115
YES
NO
END
OUTPUT REDUNDANCY ADDRESS FOR EACH CHIP
S116

FIG. 23

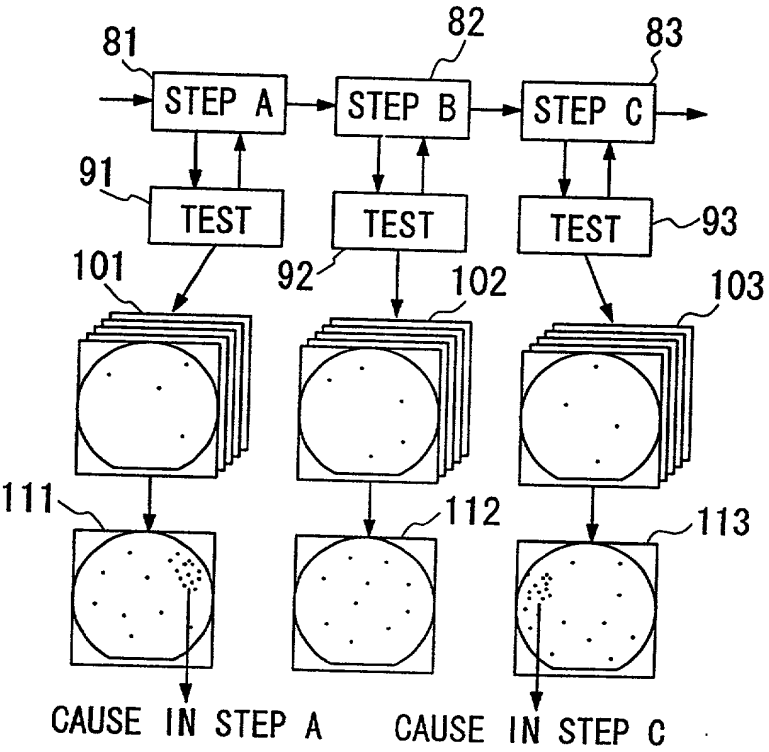

81
82
83
STEP A
STEP B
STEP C
91
TEST
TEST
TEST
93
101
92
102
103
111
112
113
CAUSE IN STEP A
CAUSE IN STEP C

FIG. 24

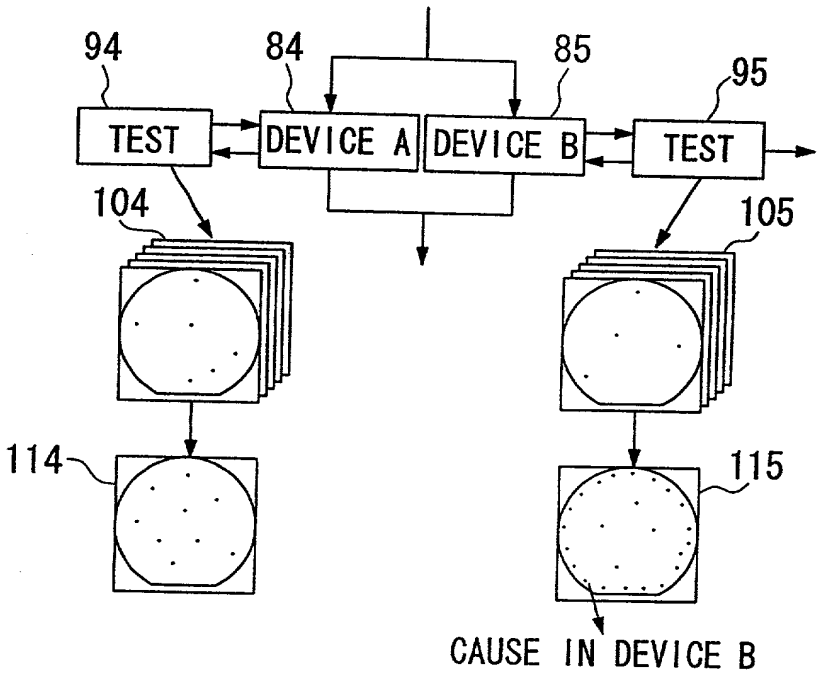

94
84
85
95
TEST
DEVICE A
DEVICE B
TEST
104
105
114
115
CAUSE IN DEVICE B

FIG. 25

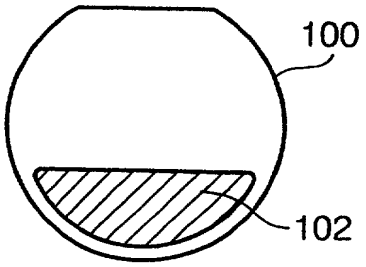


FIG. 26

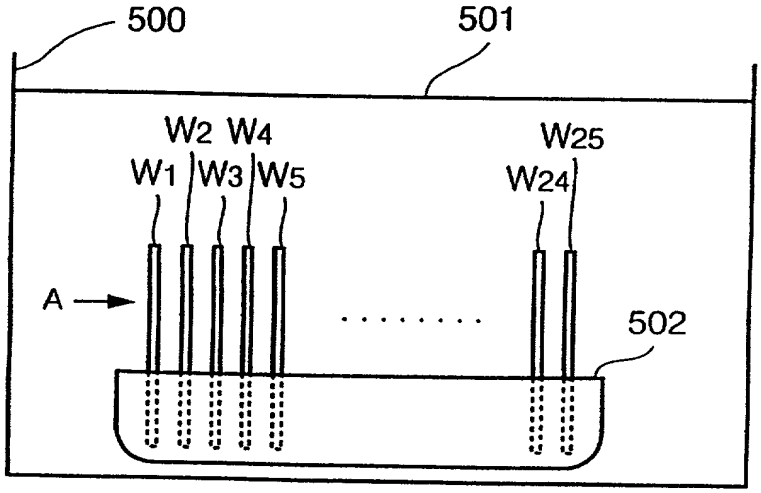


FIG. 27